<u>IN THE SPECIFICATION</u>

On page 10, lines 20 –25, and on page 11, lines 1-7, please replace the original paragraph with the following:

Figure 3A illustrates an exemplary layout of a T4 driver. The driver includes twelve transistors T1 to T12 ~~390~~ arranged symmetrically along four legs 310-325. The legs 310-325 are arranged in a bilaterally symmetric format. The legs 310-325 form the gates of transistors T1 340 to T12 ~~395~~. For one embodiment, the legs 310-325 are polysilicon. Alternatively, the legs 310-325 may be metal, or another conductive material. The legs 310-325 are placed on a substrate (not shown). The substrate includes source 330 and drain sections 340, in an alternating pattern. Thus, for example, all corners and the center section may be source sections 330, while the other sections are drain sections 340. Around each crossing of the legs 310-320 is a non-diffused area 350. The interconnections between the sources are not shown. For one embodiment, the sources may be tied together and the drains may be tied together, using metal layers.

On page 11, lines 8-14, please replace the original paragraph with the following:

Thus, for example, one transistor, T1 ~~360~~ 390, is circled, including a portion of leg 310 and adjacent source 330 and drain 340 areas. Transistor T1 ~~360~~ 390 shares a source with transistor T8, and a drain with transistor T2. The gate area of the transistor T1 ~~360~~ 390 is defined by the edge of the structure and the non-diffused area 350. Figures 3B and 3C illustrate permutations of this design, with fewer numbers of

transistors. Similarly, additional transistors may be added to the system, while

balancing the number of transistors.